

291.7957 -63.1

Bild 2-14 Meßaufbau

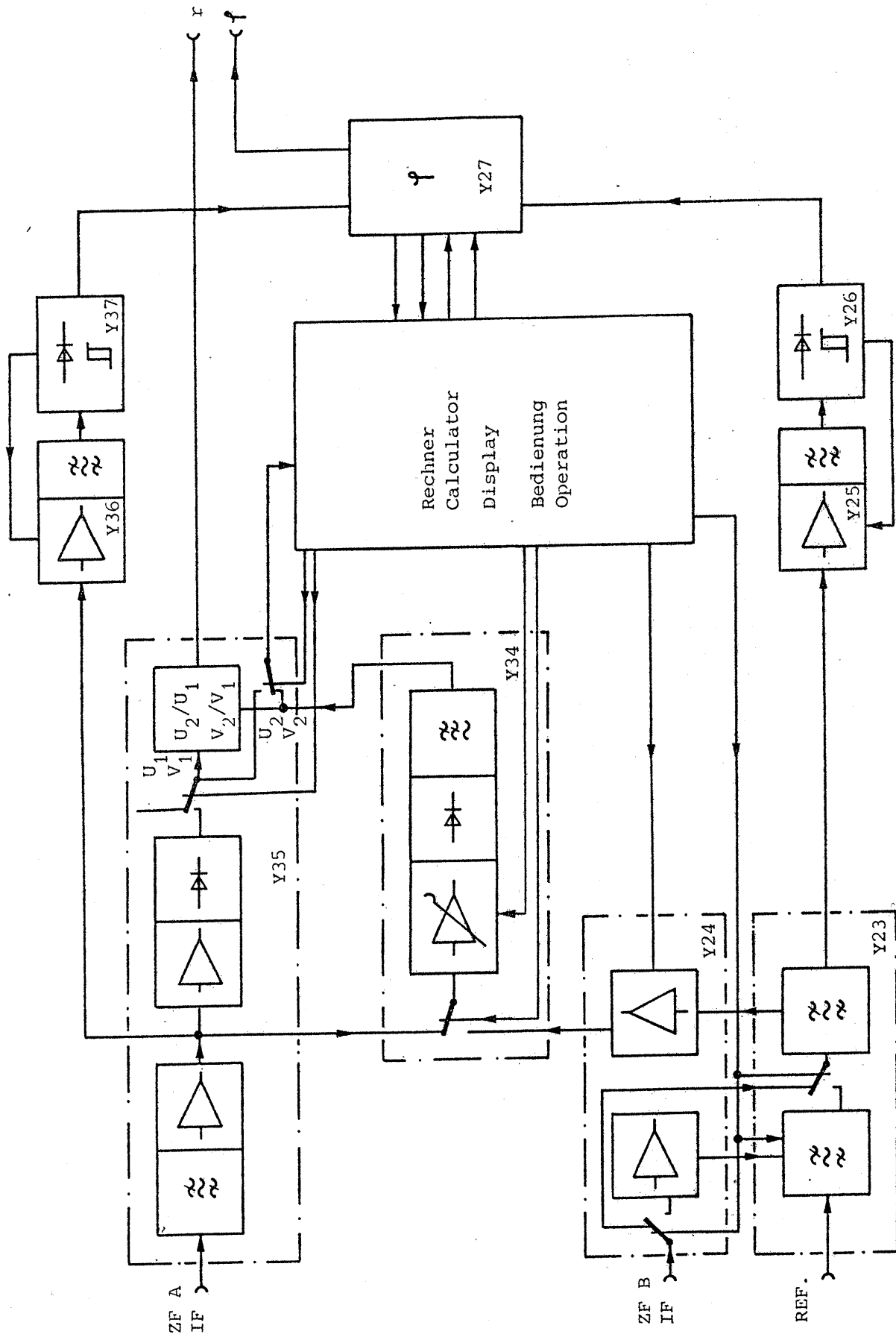


Bild 4-1 Blockschaltbild des ZPV
 Fig. 4-1 Block diagram of ZPV

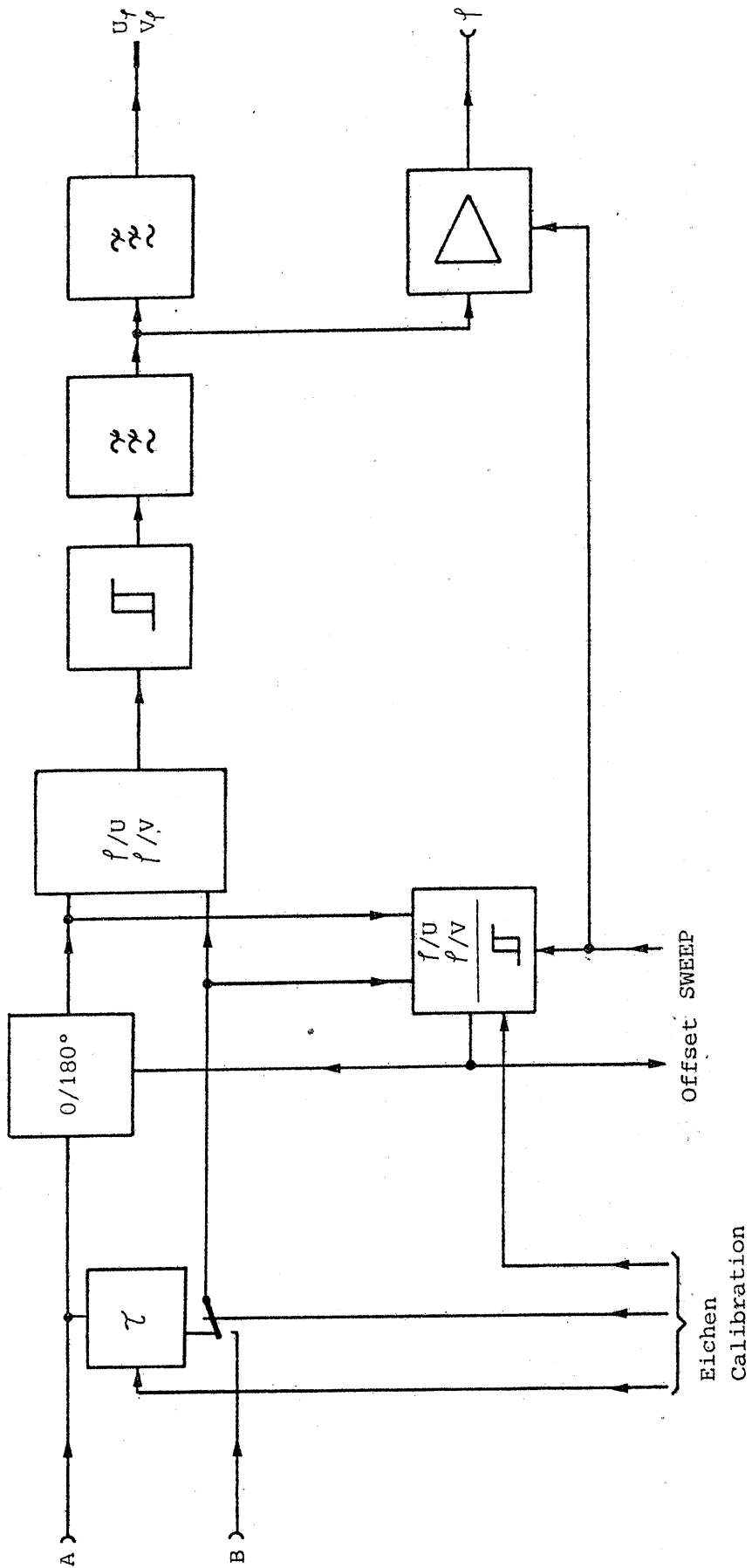


Bild 4-2 Blockschaltbild der Phasenanzeige Y27
 Fig. 4-2 Block diagram of phase indication Y27

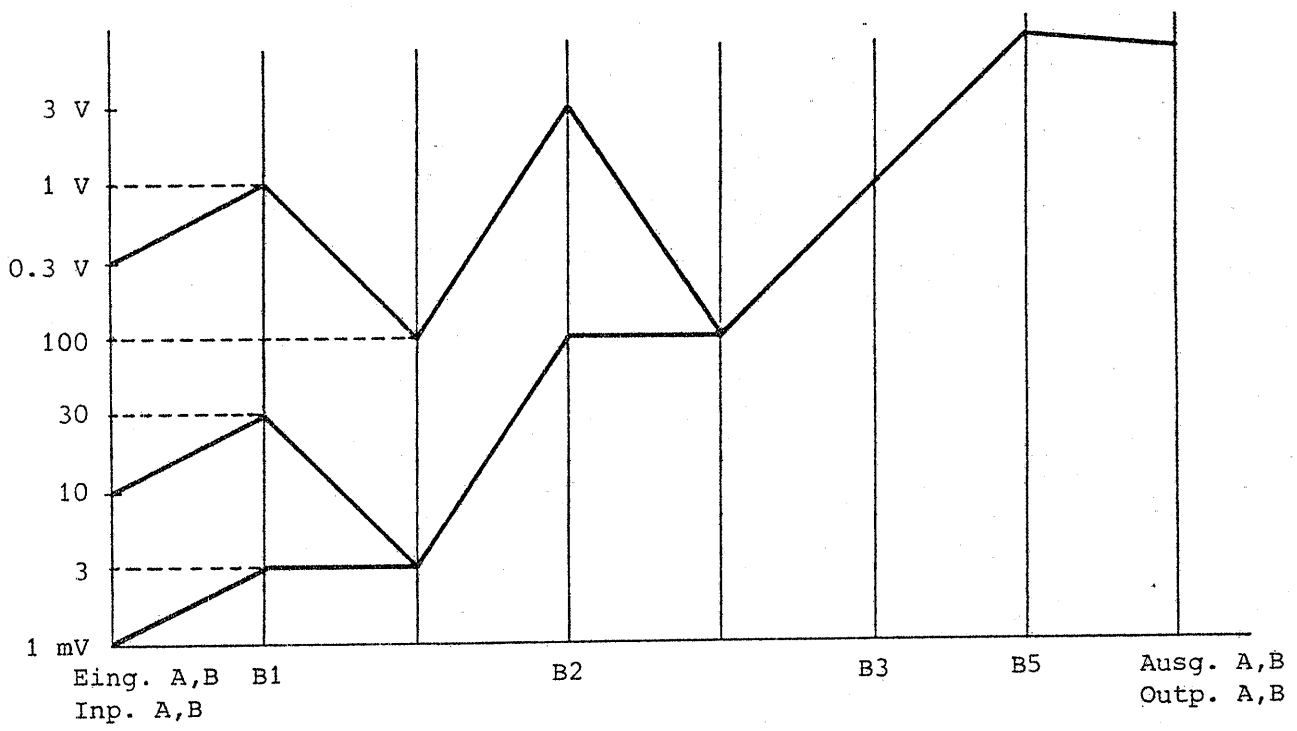


Bild 4-3 Pegelplan der Amplitudenanzeige Y34
 Fig. 4-3 Level diagram of amplitude indication Y34

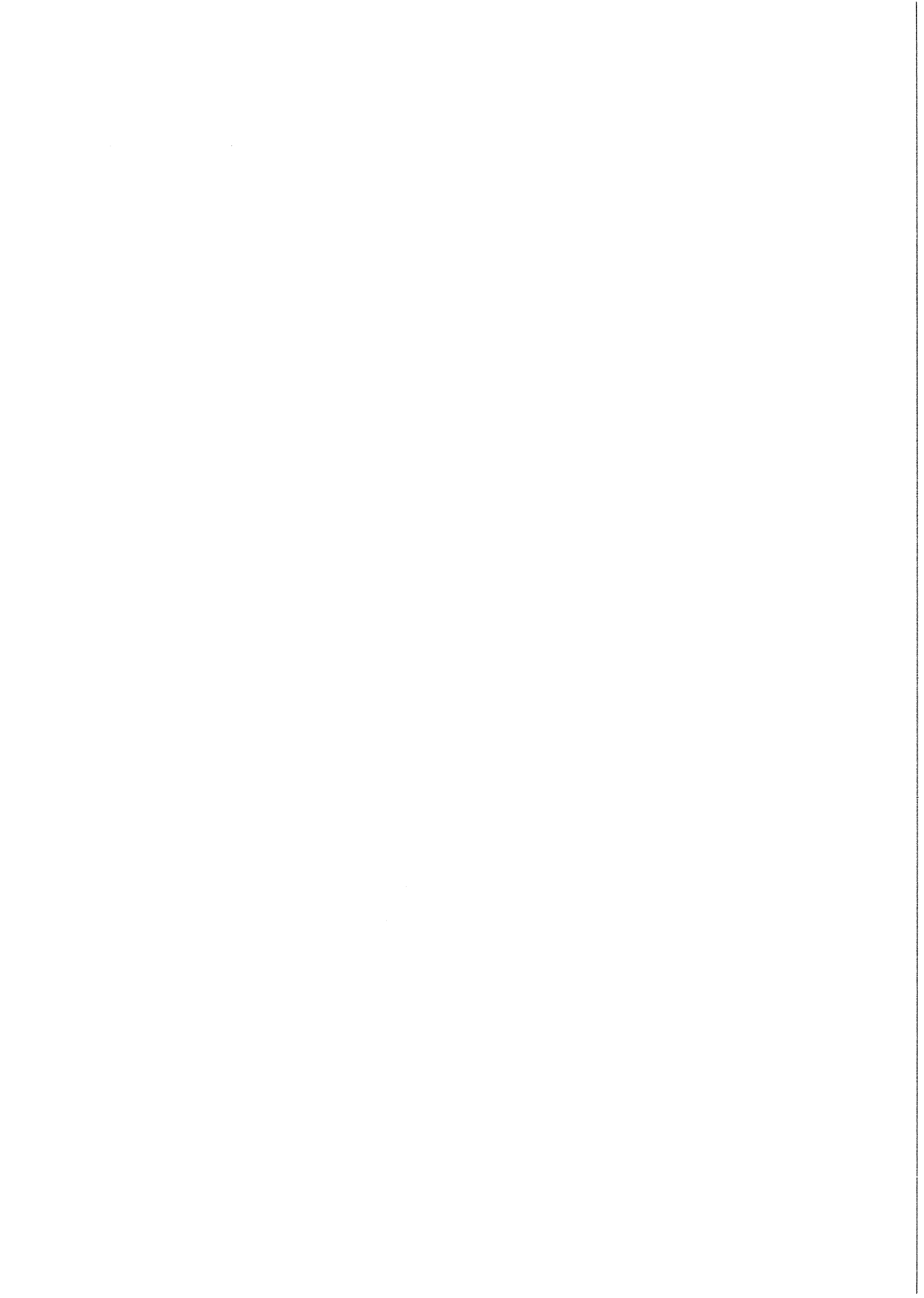
Amplitudenanzeige Y34 Amplitude indication						Vorverstärker B Y24 Pre-Amplifier B	
BU34.7b Kanal/Channel		Meßbereich Measuring range	BU34.8	.9	.10	BU24.31a	.11a
B	A		R0	R1	R2	R3	R4
1	0	1000 mV	1	0	1	1	0
1	0	300 mV	1	1	1	1	0
1	0	100 mV	0	0	1	1	0
1	0	30 mV	1	0	0	1	0
1	0	10 mV	1	1	0	1	0
1	0	3 mV	0	0	0	1	0
1	0	1 mV	0	1	0	1	0
1	0	0,3 mV	0	0	0	0	0
1	0	100 µV	1	0	0	1	1
1	0	30 µV	1	1	0	1	1

0 $\hat{=}$ 0 V
1 $\hat{=}$ +5 V

Tabelle 4-4 Steuersignale für Kanalumschaltung und Bereichswahl
Table 4-4 Control signals for channel and range selection

Selektion A Selection A Y35	EIN ON	AUS OFF	
Bandbreite A (2 kHz) BU35.2b Bandwidth A	0	1	
SBW-INP. (SWEEP) BU35.2a	0	1	
B/A (SWEEP) BU35.1b	0	1	0 $\hat{=}$ 0 V
A, B (SWEEP) BU35.1b	1	0	1 $\hat{=}$ +5 V

Tabelle 4-5 Steuersignale für SWEEP-Umschaltung
Table 4-5 Control signals for SWEEP selection



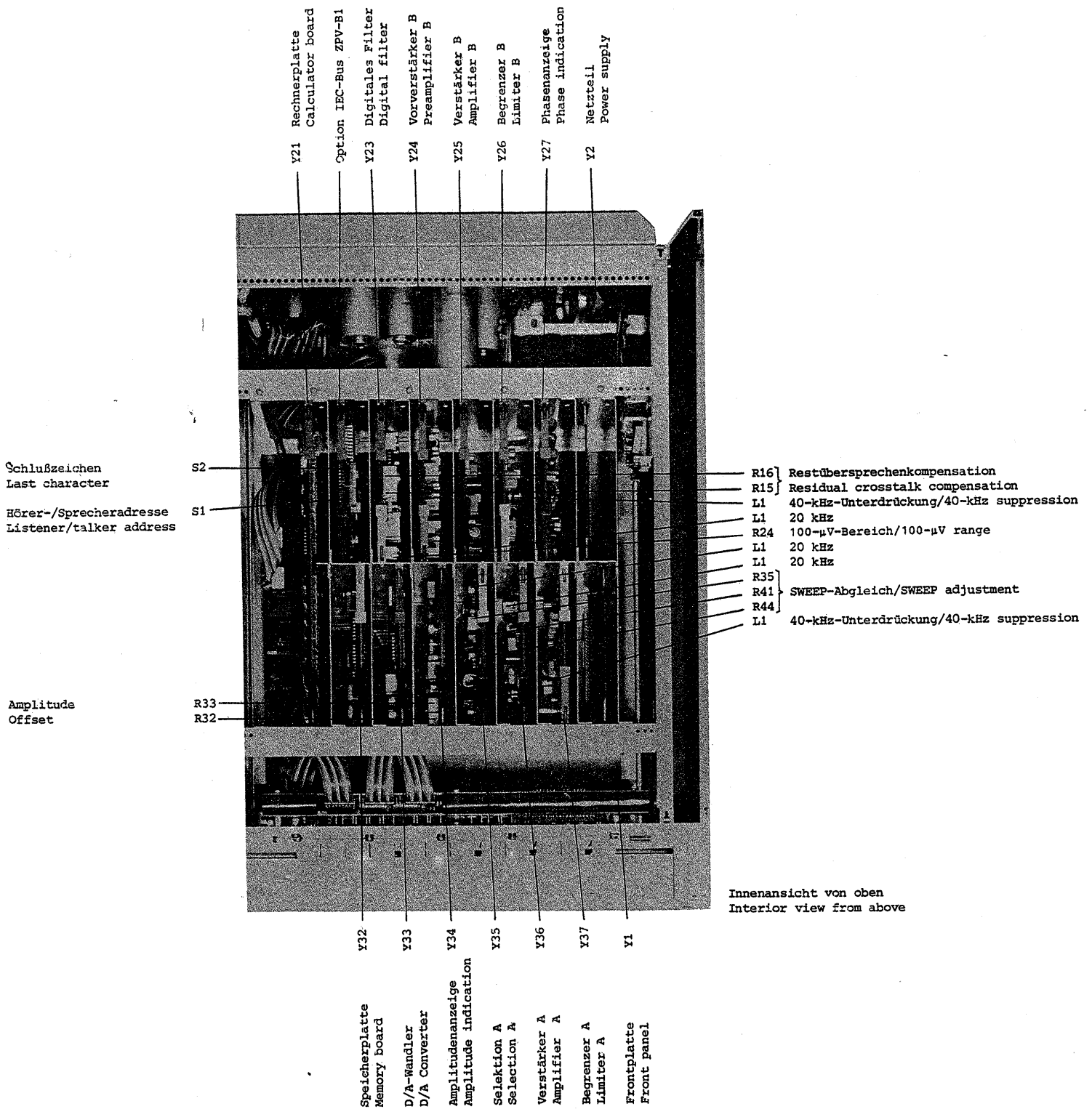
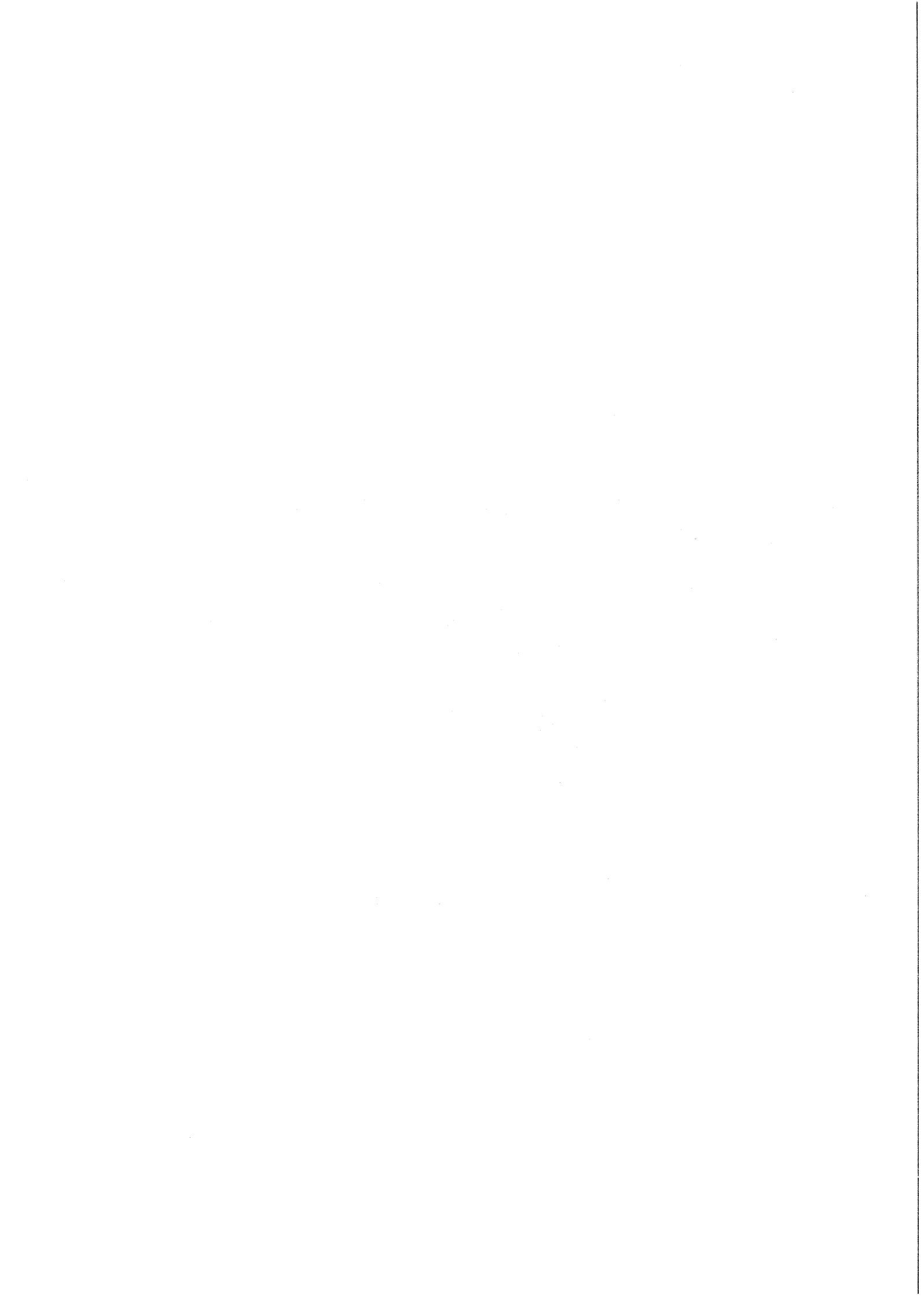


Bild 5-1 Lage der Baugruppen und Abgleichelemente
Fig. 5-1 Location of modules and adjusting elements



Messung Measurement	Meßpunkt Rechnerplatte Checkpoint Computer board	Signatur/Signature			
		ohne Optionen W/o options	mit Opt. with opt. B2	mit Opt. with opt. B3	mit Opt. with opt. B2+B3
DB0	ST9.1	PHAO	8UOF	7A87	182C
DB1	ST8.1	7783	7P9H	CA11	C30U
DB2	ST6.1	05H8	H682	9264	413P
DB3	ST4.1	UUP6	C535	574C	1H98
DB4	ST5.1	2U82	5F68	2413	57U9
DB5	ST10.1	760P	1344	9F9A	U4HO
DB6	ST7.1	6P24	P2HA	F45P	48A0
DB7	ST11.1	A50P	8145	1PUC	3ACO
+5 V		755U	755U	755U	755U

Tabelle 5-1
Table 5-1

start  Stop  Clock 

Messung Measurement	Meßpunkt Checkpoint		Signatur Signature
	Rechnerplatte Computer board	Speicherplatte Memory board	
A0	B3.25, B4.2		H335
A1	B3.26, B4.4		C113
A2	B3.27, B4.6		7050
A3	B3.29, B4.8		0772
A4	B3.30, B4.10		C4C3
A5	B3.31, B4.12		AA08
A6	B3.32, B5.4		7211
A7	B3.33, B5.6		A3C1
A8	B3.34, B5.10		7707
A9	B3.35, B5.8		577A
A10	B3.1, B5.12		HH86
A11	B3.40, B25.8		89F1
A12	B3.37, B25.12		AC99
A13	B3.38, B25.2		PCF3
A14	B3.39		1180
A15	B3.36		0000
CS11	B11.18, B11.20		4CP2
CS13	B13.18, B13.20		U697
CS14	B14.18, B14.20		723A
CS2		B2.18, B2.20	9C54
CS3		B3.18, B3.20	18F8
CS4		B4.18, B4.20	63U6
CS5		B5.18, B5.20	A030
CS6		B6.18, B6.20	3POC
CS7		B7.18, B7.20	160P
ROM-Enable	B19.11	B1.12	0000
$\overline{\text{MEMR}}$	B6.24, B19.12		0000
A12 A13	B19.3, B19.4		6854

Tabèllle 5-2
Table 5-2

start  Stop  Clock 

Zu prüfendes ROM ROM to be checked		Signal							
auf Rechnerplatte on computer board	auf Speicherplatte on memory board	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7
B11		1U1F	C642	64UA	0CUA	48CF	FPA5	A7F1	A52P
B13		17U3	7F41	A605	3U8F	Q6C5	1H15	U9A1	5114
B14		P278	C8FH	P2P3	HHU2	7PFP	92FC	HU25	FPAA
	B2	PPP3	94UH	3012	7UC5	1071	F755	92PH	FA3A
	B3	1788	A306	1PC5	6713	1P70	97CA	HF25	F05C
	B4	082P	U4CC	0C32	340P	4AHC	8260	H55U	410H
	B5	6875	300A	5P3U	8PH4	PAUH	FU07	1H93	FC43
	B6	F51F	37H4	UOPP	7U35	7122	58P6	3960	2471
	B7	AP90	Q5PU	PA66	2U35	C836	UOF5	7681	A47P

Tabelle 5-3
Table 5-3

